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(54) Abstract Title
Telecommunications system

(57) An air frame synchronisation signal is transmitted as a data signal over a PCM link from a central unit 2 to a plurality of remote radio basestation transceivers 10, allowing the remote radio basestation transceivers to recreate the AFS signal with the desired accuracy, compensating for transmission delays.

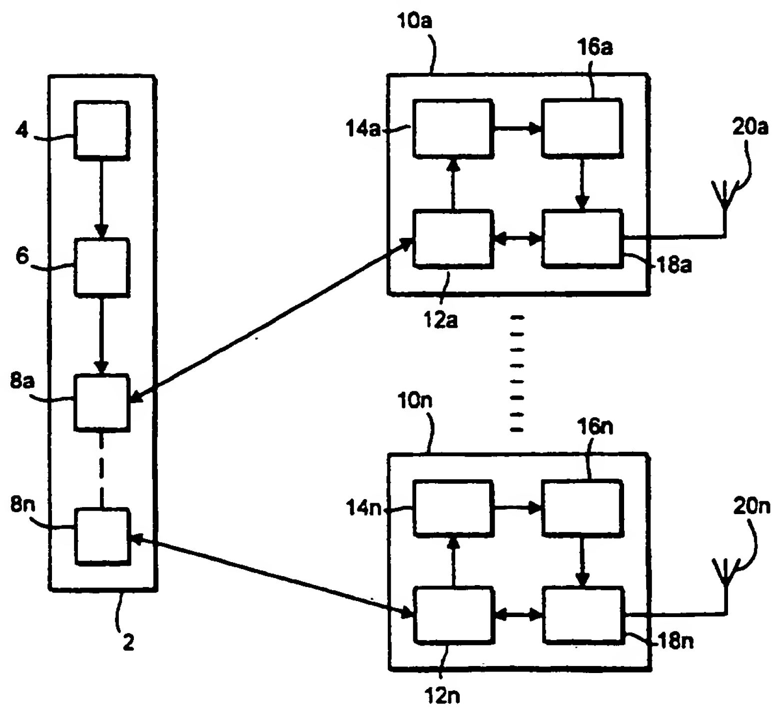

FIG. 1

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TELECOMMUNICATIONS SYSTEM

TECHNICAL FIELD OF THE INVENTION

This invention relates to a telecommunications system, and in particular to a network comprising a base station with a control unit and a plurality of remote radio transceivers and to a method of establishing air frame synchronisation between the remote radio transceivers.

DESCRIPTION OF RELATED ART

A conventional digital cellular telephone base station includes a large number of radio transceivers, typically controlled from a central unit. Transmissions from the radio transceivers are divided into frames, and each frame contains a plurality of time slots, which typically contain transmissions to different mobile transceivers. A time division multiplex (TDM) link is used for carrying control and traffic signals between the control unit and the remote radio transceivers.

It is known to synchronise the radio transceivers, so that each radio transceiver begins transmission of a new frame at the same moment. In a conventional network, air frame synchronisation between the radio transceivers is established by means of a central timing unit, which is connected to all of the radio transceivers via a local bus cable network, and transmits a signal at 25Hz, which is the air frame rate, to the radio transceivers.

However, this method of distributing the air frame synchronisation signals is disadvantageous when the radio transceivers are at a significant distance, for example up to 1,000m, from the central timing unit, since then the propagation delays along the cable mean that true synchronisation can be lost and a separate cable is necessary for the air frame synchronisation

signal.

SUMMARY OF THE INVENTION

The present invention seeks to provide a method of distributing air frame synchronisation between widely spaced radio transceivers, without requiring additional infrastructure.

In preferred aspects of the present invention, the air frame synchronisation signal is transmitted to the remote radio transceivers on the TDM link which carries the traffic and control signals. Preferably, data relating to the air frame synchronisation signal is encoded and transmitted in a time slot on the TDM link, and each remote radio transceiver includes circuitry for regenerating the air frame signal from the transmitted data.

Preferably, also, the remote radio transceiver includes circuitry for compensating for any delays on the transmission link.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic representation of a network in accordance with the invention.

Figure 2 is a schematic block diagram of a part of the central unit in the network.

Figure 3 is a timing diagram illustrating the invention.

Figure 4 is a schematic diagram of a part of a base station.

Figure 5 represents the delays which occur when transmitting signals in the network.

Figure 6 further represents the delays which occur when transmitting signals in the network.

Figure 7 is a timing diagram illustrating an aspect of the invention.

Figure 8 is a schematic diagram of a part of a remote radio transceiver.

Figure 9 is a schematic diagram of a further part of a remote radio transceiver.

Figure 10 is a schematic diagram of a still further part of a remote radio transceiver.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

Figure 1 is a schematic representation of a network in accordance with the invention. A central unit 2 comprises a master air frame synchronisation (AFS) oscillator 4, which is connected to an AFS digital encoder block 6, which in turn is connected to a plurality of digital interfaces 8a, ..., 8n. Each of the digital interfaces is connected over a respective TDM (or time division multiplexed) link, also referred to herein as a pulse code modulated (or PCM) link, to a respective remote radio transceiver 10a, ... 10n. Each remote radio transceiver comprises a respective digital interface 12a, ..., 12n, which is connected to an AFS digital decoder block 14a, ..., 14n, which in turn is connected to a slave AFS oscillator 16a, ..., 16n. The digital interface 12a, ..., 12n is also connected to a radio transceiver 18a, ..., 18n, which in turn is connected to an antenna 20a, ..., 20n. The AFS oscillators 16a, ..., 16n are also connected to feed their outputs to the respective radio transceivers 18a, ..., 18n.

In the central unit 2, the master AFS oscillator 4 is conventional, and will not be described further herein. Similarly, the digital interfaces 8a, ..., 8n are conventional, and will not be described further.

In accordance with the invention, the AFS encoder 6 is responsible for generating data relating to the phase of the AFS signal, relative to the frames of data sent from the interfaces 8a, ..., 8n to the respective remote radio transceivers 10a, ..., 10n. This encoded data is then sent to a framer via, in this specific

arrangement, a processor (not shown), which incorporates the data into the signals being transmitted on the respective PCM links. In other implementations of the invention a processor would not be required.

Specifically, with the AFS oscillator 4 being run from a 19.44MHz clock, the encoder 6 is responsible for measuring the number of these 19.44MHz cycles that separate the beginning of an AFS frame from the beginning of one of the frames in the signals sent on the PCM link.

Figure 2 is a block diagram of the AFS encoder 6.

The AFS encoder 6 receives an input TSYNC, which is an 8kHz signal derived from the transmit clock and is coincident with the start of the TDM frame. The signal TSYNC is sent to a rising edge detector 50, which generates pulses on the rising edges of the signal TSYNC. Each pulse is sent to a 12 bit AFS up counter 52. The AFS counter 52 is run from the 19.44MHz clock, and counts the number of clock cycles since its last reset. The counter 52 is reset by every pulse from the edge detector 50. A shift register 54 receives a latch input AFS strobe, which is generated by the falling edges of the 25Hz AFS signal. When an AFS strobe occurs, the count from the AFS counter 52, which is the counted number of 19.44MHz clock cycles since the beginning of a PCM frame until the beginning of an AFS frame, is latched into the 12 bit shift register 54. This count is referred to as the air frame offset. The PCM frame in which this occurs is considered frame 0 and a modulo 320 frame counter 56 is set to 1 at the next TSYNC pulse, and counts each subsequent pulse.

After the AFS count is latched into the shift register 54, a shift control counter 58 shifts the AFS

count value through a CRC4 encoder 60. After 16 shifts (12 bits of the AFS count and 4 zeros) the CRC value is available from the CRC encoder. When the frame counter 56 reaches 314, an interrupt is generated by an interrupt generator 62 at the very end of frame 314. The processor (not shown) then reads the most significant byte, referred to below as "B", of the 12 bit value from the shift register 54 via a multiplexer 64, which is controlled by decoding the frame count from the frame counter 56. The processor writes the value read from the multiplexer 64 to the transmit idle definition register of a Dallas 2151 DS1 framer which will transmit this byte in a separate AFS time slot (e.g. time slot 1) of the next frame (frame 316). Another interrupt is generated by the interrupt generator 62 at the end of frame 315. This interrupt causes the processor to read the least significant 4 bits of the data stored in the shift register 54 and the 4 bit CRC (cyclic redundancy check) value, together referred to below as the byte "C", via the multiplexer 64, and writes it to the idle definition register of the framer. A third interrupt is generated at the end of frame 316. This interrupt causes an 8 bit idle code, referred to below as "A", to be read by the processor via the multiplexer 64 and written to the framer. The framer will transmit this idle code in every frame until the next AFS event.

Figure 3 illustrates, in the top line marked XLI, the AFS data transmitted on the PCM link. As is conventional, transmissions on the PCM link are divided into a succession of frames, and each frame is divided into 24 time slots. In this case, the first time slot carries the AFS data, and is referred to as the AFS time slot.

As mentioned previously, the frame rate on the PCM

link is 8kHz, while the AFS frequency is 25Hz. Thus, there is one AFS cycle every 320 PCM frames. The beginning of an AFS cycle is referred to as AFS frame time zero, and is the point in time at which an AFS Strobe signal occurs, and it is at this point that the value from the AFS counter 52 is latched into the shift register 54. The PCM frame during which this occurs is referred to as frame 0. As discussed above, idle codes "A" are transmitted during the AFS time slots of each of frames 1-315. Then, the most significant byte "B" is transmitted during the AFS time slot of frame 316, and the least significant byte "C" is transmitted during frame 317. Idle codes "A" are then transmitted during the remaining frames until the cycle repeats.

As shown in the lower line marked RXLI of Figure 3, signals transmitted on the PCM link are received at the relevant remote radio transceiver after a time delay, which depends amongst other things on the physical separation of the remote radio transceiver from the central unit. To ensure that all of the remote radio transceivers are accurately synchronised with one another, and with the AFS signal generated in the central unit, it is necessary to compensate in each radio transceiver for the respective time delays. As a result of these time delays, the bytes "B" and "C" are transmitted on the PCM link several frames before the next AFS frame time zero, and the receiving remote radio transceiver is then able to act on the received data by generating its own AFS, with a frame time zero at a point determined by a known transmission delay, taking into account the measured time by which the transmission of bytes "B" and "C" precede the beginning of the new frame 0, and the transmitted data which relates to the time difference between the beginning of frame 0 and the required AFS frame time zero.

The transmit delay is approximately 16μs for a cable length of 0, and 23μs at a cable length of 1,000m.

Moreover, there are delays once the signal has reached the remote radio transceiver, due to the presence of an elastic store (as described hereafter), which can introduce a delay of up to two TDM frames.

In this illustrated embodiment, the expected time delays are such that it is sufficient to send bytes "B" and "C" in frames 316 and 317, as this gives sufficient time for the receiving remote radio transceiver to act on the received data, even with the longest conceivable transmission delays. In networks which might have longer transmission delays, it might be necessary to transmit the AFS data earlier in the cycle.

In regenerating the AFS signal, the remote radio transceiver uses the middle of frame 317, in which the second byte "C" of the AFS data is received, as its reference point. From this point, the base station counts 312.5μs (equivalent to two and a half TDM frames, i.e. the separation of the reference point from the beginning of frame 0), plus the time determined by the decoded AFS data, minus a transmission delay factor, and minus the elastic store depth. The remote radio transceiver must also compensate for the startup delay required to resynchronise the AFS generator after a signal is sent to it.

Figure 4 shows the circuitry present in the remote radio transceiver for compensating for the transmission delay and the elastic store depth.

This circuit uses inputs which are determined by the network parameters.

Figure 5 illustrates the way in which the transmission delay is determined. A signal is sent from the remote radio transceiver, marked RXLI, over

the transmission line to the central unit, marked XLI, which is placed in loopback mode, so that the same signal is received again at the remote radio transceiver. The remote radio transceiver then measures the time taken for the round trip.

In Figure 5:

Δt_{TL} = Delay from TSYNC to Line

Δt_{L} = Propagation Delay of Line

Δt_{LR} = Delay from Line to RLCLK, where RLCLK marks the receive TDM frame boundary before the elastic store as described later

Δt_{LB} = Loopback Delay

Δt_{L} depends on the distance between the central unit and the remote radio transceiver, but the other parameters are fixed by the network hardware. The fixed delays (measured for Dallas 2151) are:

$\Delta t_{TL} = 6.88\mu s$

$\Delta t_{LR} = 9.48\mu s$

$\Delta t_{LB} = 1.38\mu s$

The remote radio transceiver RXLI can only make a round trip measurement. As can be seen from Figure 5, this takes a time $\Delta t_{Round\ Trip}$, given by:

$$\Delta t_{Round\ Trip} = \Delta t_{TL} + \Delta t_{L} + \Delta t_{LB} + \Delta t_{L} + \Delta t_{LR}$$

Solving for Δt_{L}:

$$\Delta t_{L} = \tfrac{1}{2}(\Delta t_{Round\ Trip} - \Delta t_{TL} - \Delta t_{LB} - \Delta t_{LR})$$

The transmission delay factor, TxDelay, which needs to be taken into account when regenerating the AFS signal, is:

$$TxDelay = \Delta t_{TL} + \Delta t_{L} + \Delta t_{LR}$$

Substituting for Δt_{L},

$$TxDelay = \tfrac{1}{2}(\Delta t_{Round\ Trip}) + \tfrac{1}{2}(\Delta t_{TL} + \Delta t_{LR} - \Delta t_{LB})$$

Substituting for the fixed values indicated above,

$$TxDelay = \tfrac{1}{2}(\Delta t_{Round\ Trip}) + 7.49\mu s.$$

Figure 6 shows the sources of the delays which arise between the transmission of the data, and the

time when the data is received in the remote radio transceivers in a form in which it can be used. In Figure 6, Δt_{TL}, Δt_L and Δt_{LR} have the same meanings as in Figure 5, while Δt_{ES} is the elastic store delay, or elastic store depth.

The elastic store is essentially a variable depth FIFO and is used to rate adapt the 1.544Mbps PCM line data to the phase locked 2.048Mbps data rate generated at the remote radio transceiver. The elastic store depth can vary between 0 and 250μs, and cannot be forced to a known depth with the Dallas 2151 framer. In order to compensate for this variable delay, the remote radio transceiver measures the elastic store depth occurs every 24 TDM frames. The Dallas 2151 T1 framer is configured such that RSYNC occurs only at 24 TDM frames and RLCLK is high for one TDM frame. RSYNC marks the TDM frame after the elastic store. The timing relationship between RLCLK and RSYNC is shown in Figure 7.

To compensate for the elastic store depth, the term (250μs - Elastic Store Depth) is needed.

Thus, the time delay which the remote radio transceiver must apply, after receiving the transmitted data in usable form, and taking the midpoint of the frame in which the second byte "C" is received as its reference point is given by:

[62.5μs - TxDelay - 1.54μs] + [250μs - Elastic Store Depth] + Air Frame Offset

(where 1.54μs is the startup delay required to resynchronise the AFS generator).

By substituting for TxDelay, the term:

[62.5μs - TxDelay - 1.54μs], referred to herein as LC, simplifies to:

$$LC = 62.5\mu s - \tfrac{1}{2}(\Delta t_{Round\ Trip}) - 7.49\mu s - 1.54\mu s$$
$$= 53.47\mu s - \tfrac{1}{2}(\Delta t_{Round\ Trip})$$

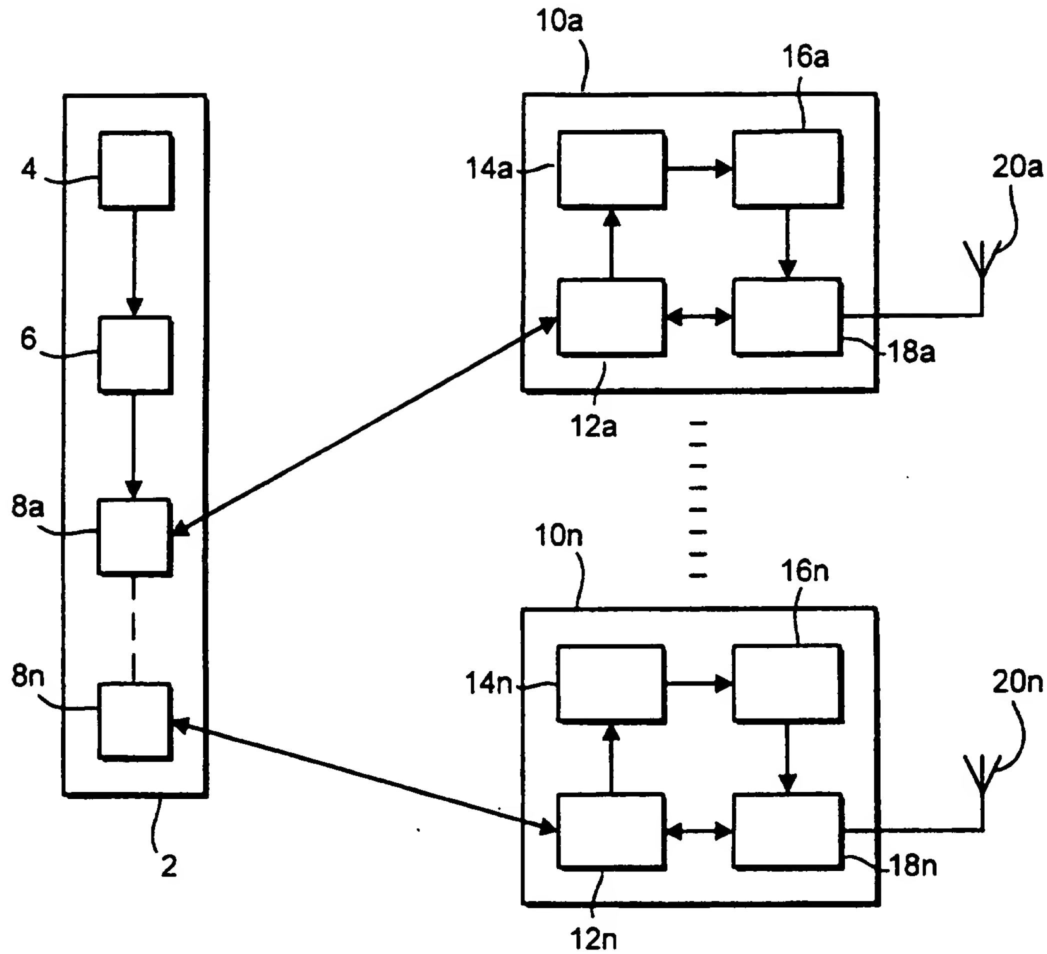


FIG. 1

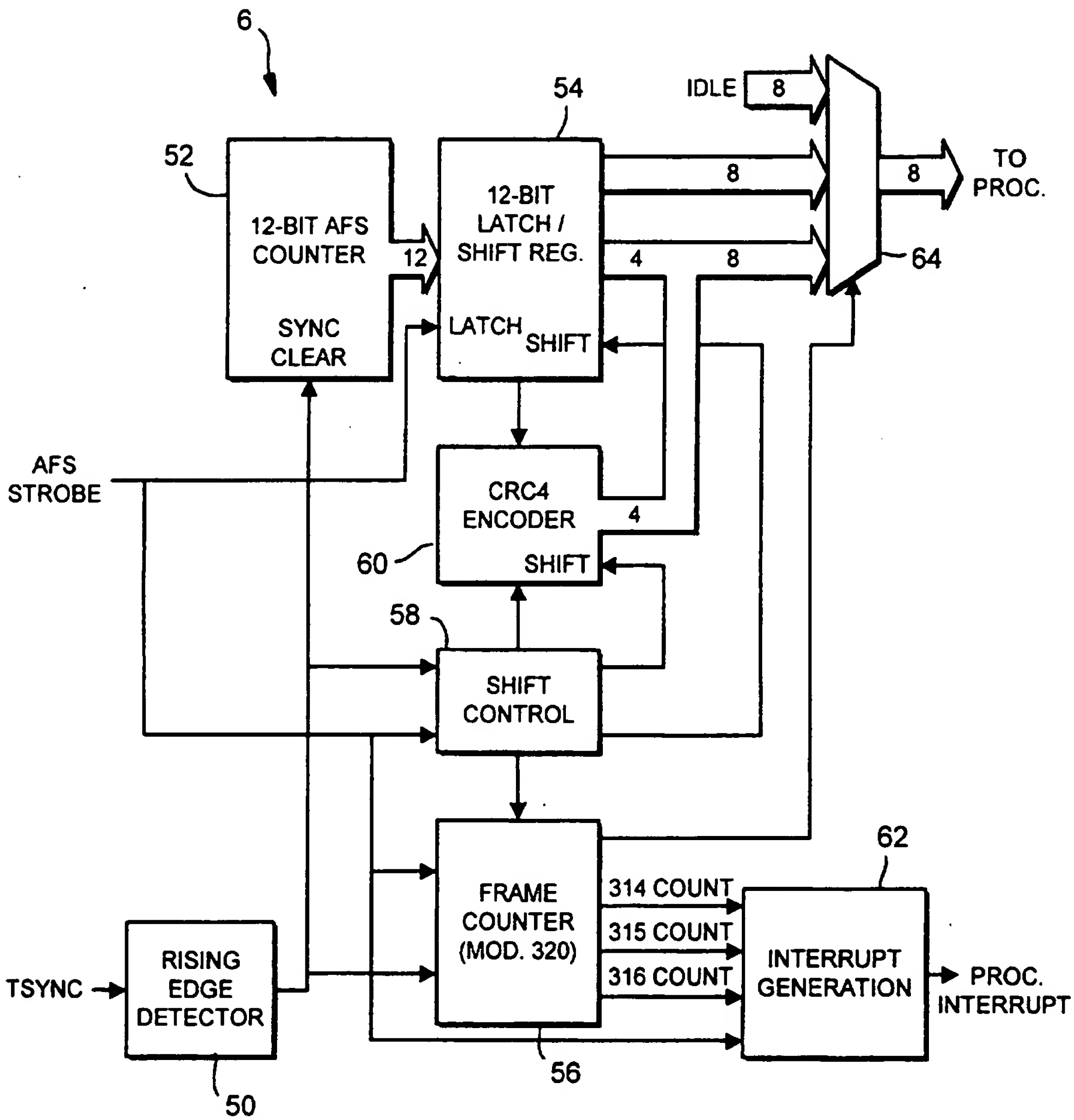
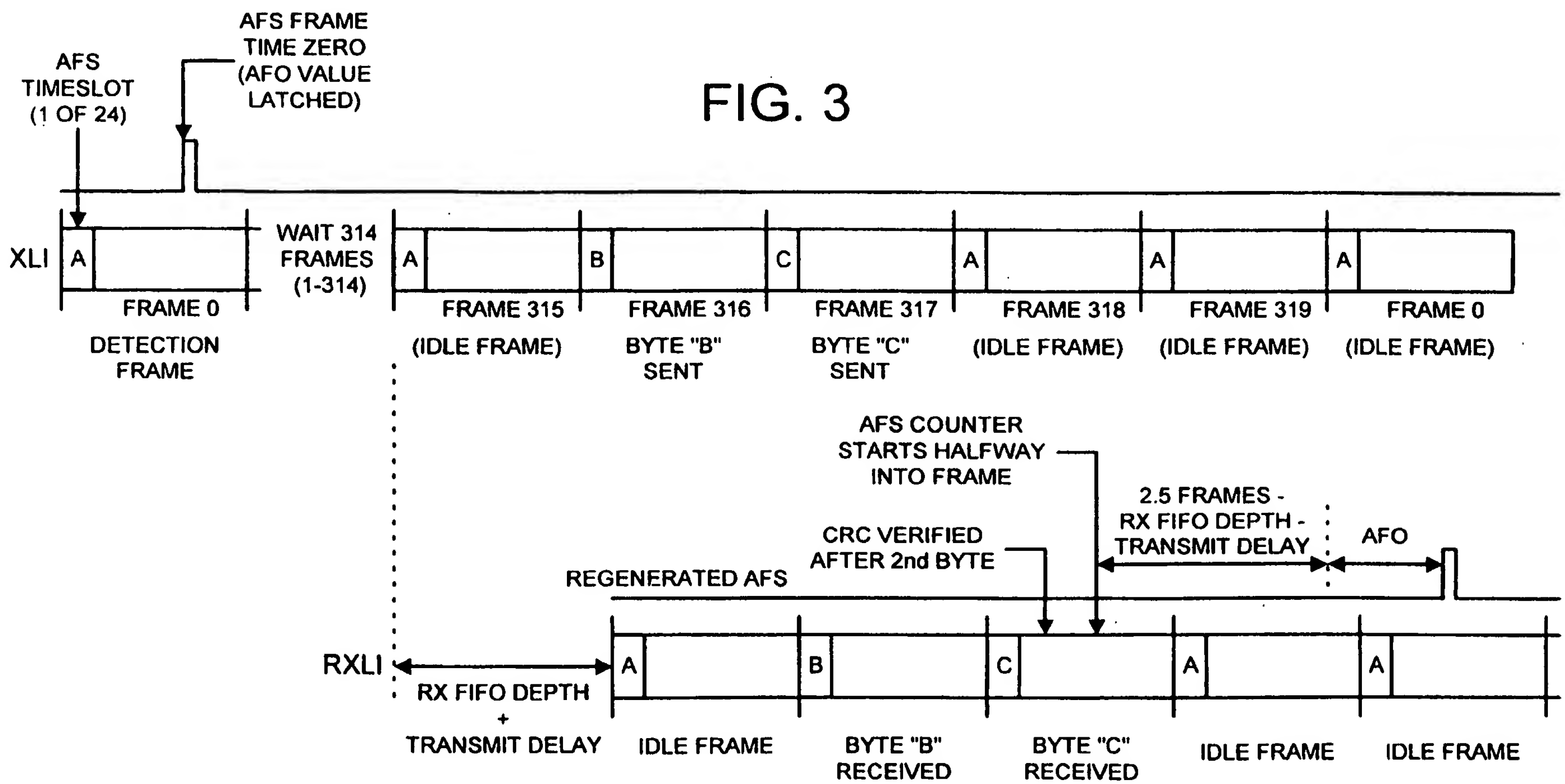

6
52
12-BIT AFS
COUNTER
SYNC
CLEAR
12
54
12-BIT
LATCH /
SHIFT REG.
LATCH
SHIFT
IDLE
8
8
8
4
8
TO
PROC.
64
AFS
STROBE
CRC4
ENCODER
4
SHIFT
60
58
SHIFT
CONTROL
FRAME
COUNTER
(MOD. 320)
314 COUNT
315 COUNT
316 COUNT
62
INTERRUPT
GENERATION
PROC.
INTERRUPT
TSYNC
RISING
EDGE
DETECTOR
50
56

FIG. 2

FIG. 3



AFS
TIMESLOT
(1 OF 24)
AFS FRAME
TIME ZERO
(AFO VALUE
LATCHED)
XLI
A
FRAME 0
DETECTION
FRAME
WAIT 314
FRAMES
(1-314)
A
FRAME 315
(IDLE FRAME)
B
FRAME 316
BYTE "B"
SENT
C
FRAME 317
BYTE "C"
SENT
A
FRAME 318
(IDLE FRAME)
A
FRAME 319
(IDLE FRAME)
A
FRAME 0
(IDLE FRAME)
AFS COUNTER
STARTS HALFWAY
INTO FRAME
2.5 FRAMES -
RX FIFO DEPTH -
TRANSMIT DELAY
AFO
CRC VERIFIED
AFTER 2nd BYTE
REGENERATED AFS
RXLI
RX FIFO DEPTH
+
TRANSMIT DELAY
A
IDLE FRAME
B
BYTE "B"
RECEIVED
C
BYTE "C"
RECEIVED
A
IDLE FRAME
A
IDLE FRAME

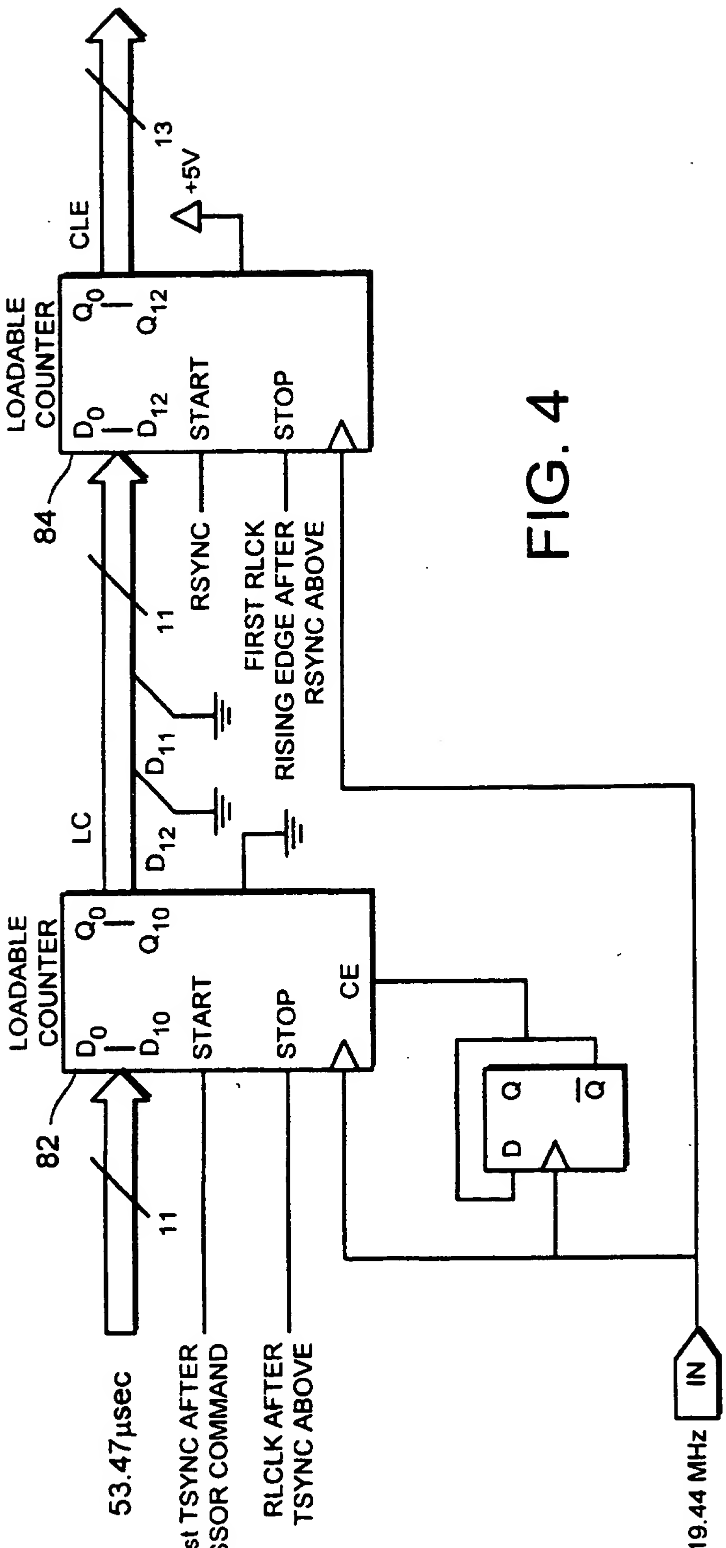

LOADABLE COUNTER
D0
D12
START
STOP
Q0
Q12
CLE
13
+5V
84
11
RSYNC
FIRST RLCK RISING EDGE AFTER RSYNC ABOVE
LC
D11
D12
LOADABLE COUNTER
D0
D10
START
STOP
CE
Q0
Q10
82
11
D
Q
Q̄
53.47µsec
1st TSYNC AFTER PROCESSOR COMMAND
RLCLK AFTER TSYNC ABOVE
IN
19.44 MHz

FIG. 4

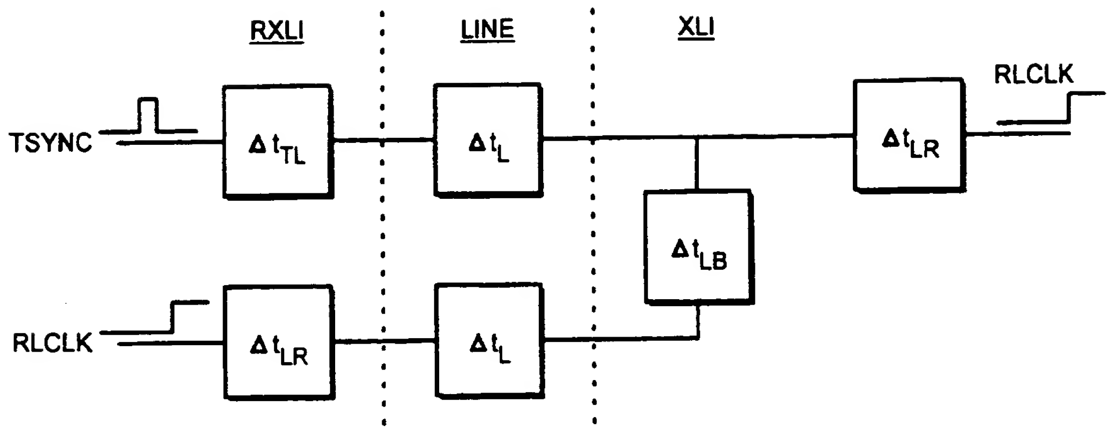


FIG. 5

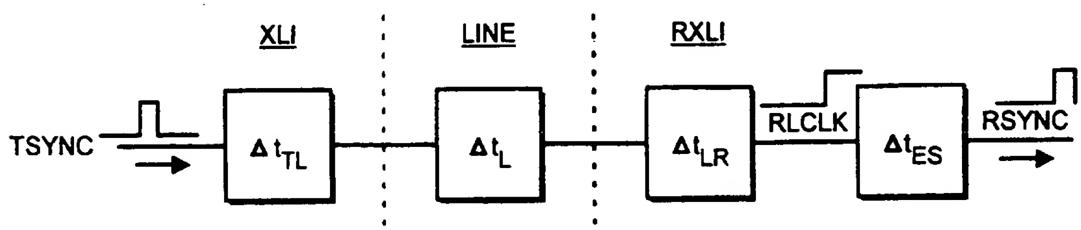


FIG. 6

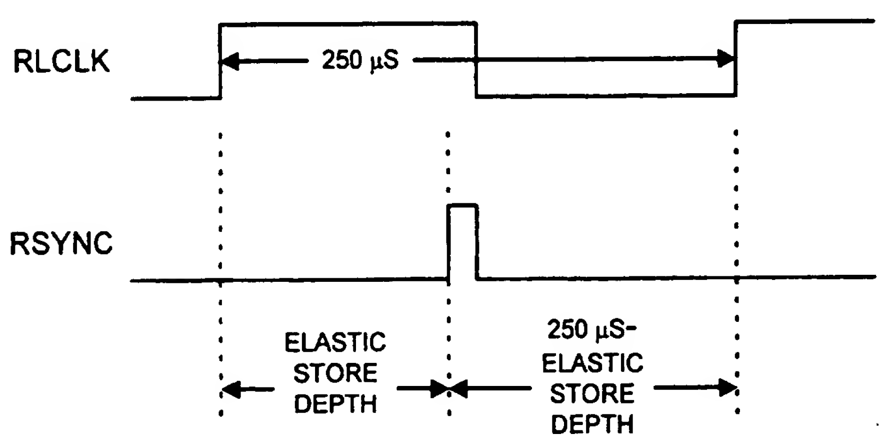


FIG. 7

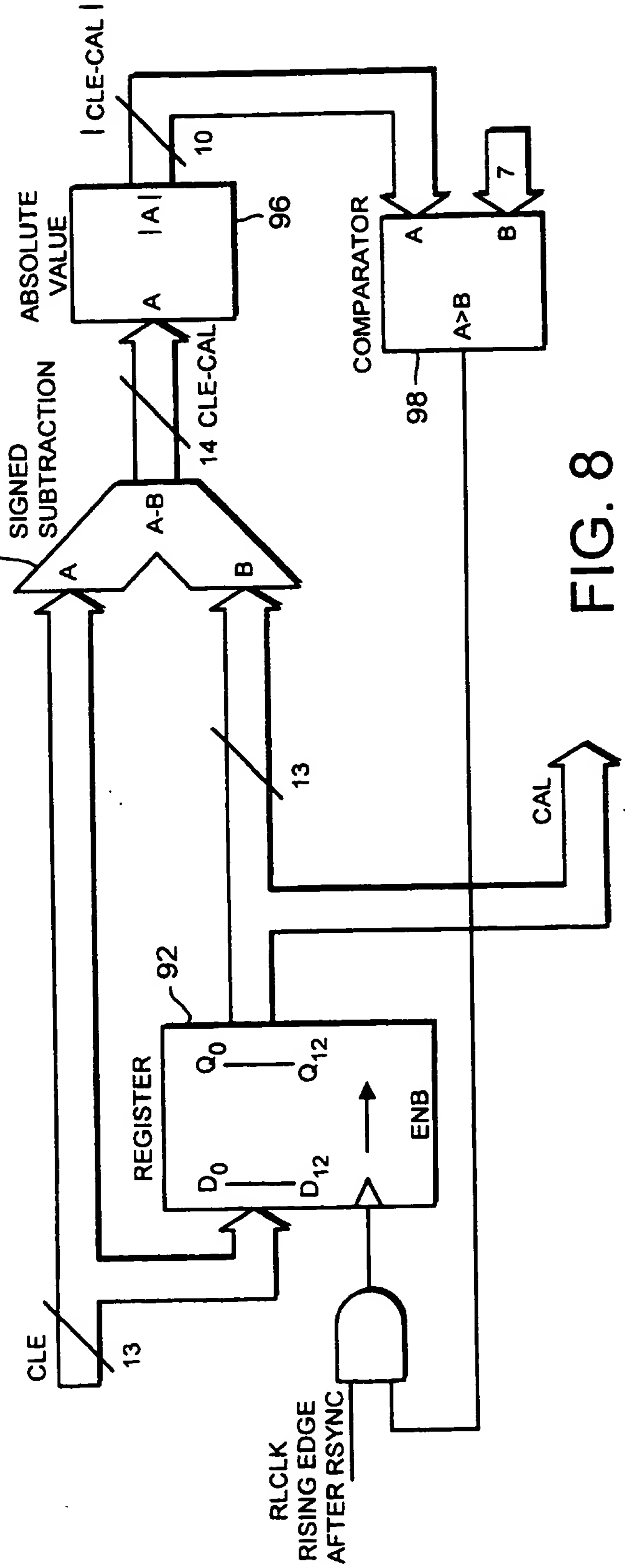
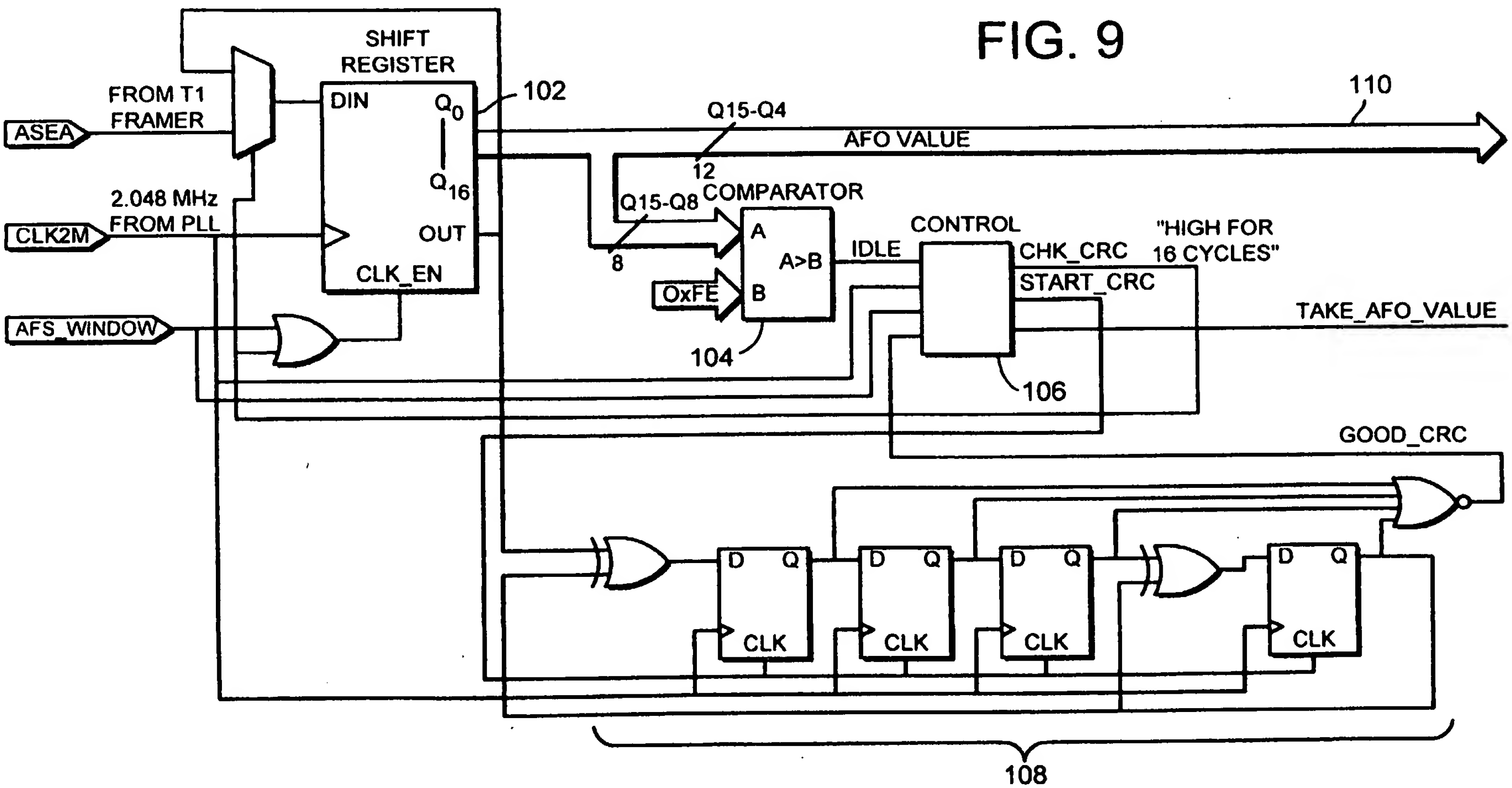

| CLE-CAL |
10
ABSOLUTE VALUE
| A |
A
96
7
COMPARATOR
A
B
A>B
98
94
SIGNED SUBTRACTION
A-B
A
B
14 CLE-CAL
13
CAL
92
REGISTER
Q_0
Q_{12}
D_0
D_{12}
ENB
CLE
13
RLCLK RISING EDGE AFTER RSYNC

FIG. 8

FIG. 9


SHIFT REGISTER
102
DIN
Q0
Q16
OUT
CLK_EN
FROM T1 FRAMER
ASEA
2.048 MHz FROM PLL
CLK2M
AFS_WINDOW
Q15-Q4
12
AFO VALUE
110
Q15-Q8
8
COMPARATOR
A
B
A>B
OxFE
104
IDLE
CONTROL
CHK_CRC
START_CRC
106
"HIGH FOR 16 CYCLES"
TAKE_AFO_VALUE
GOOD_CRC
D
Q
CLK
108

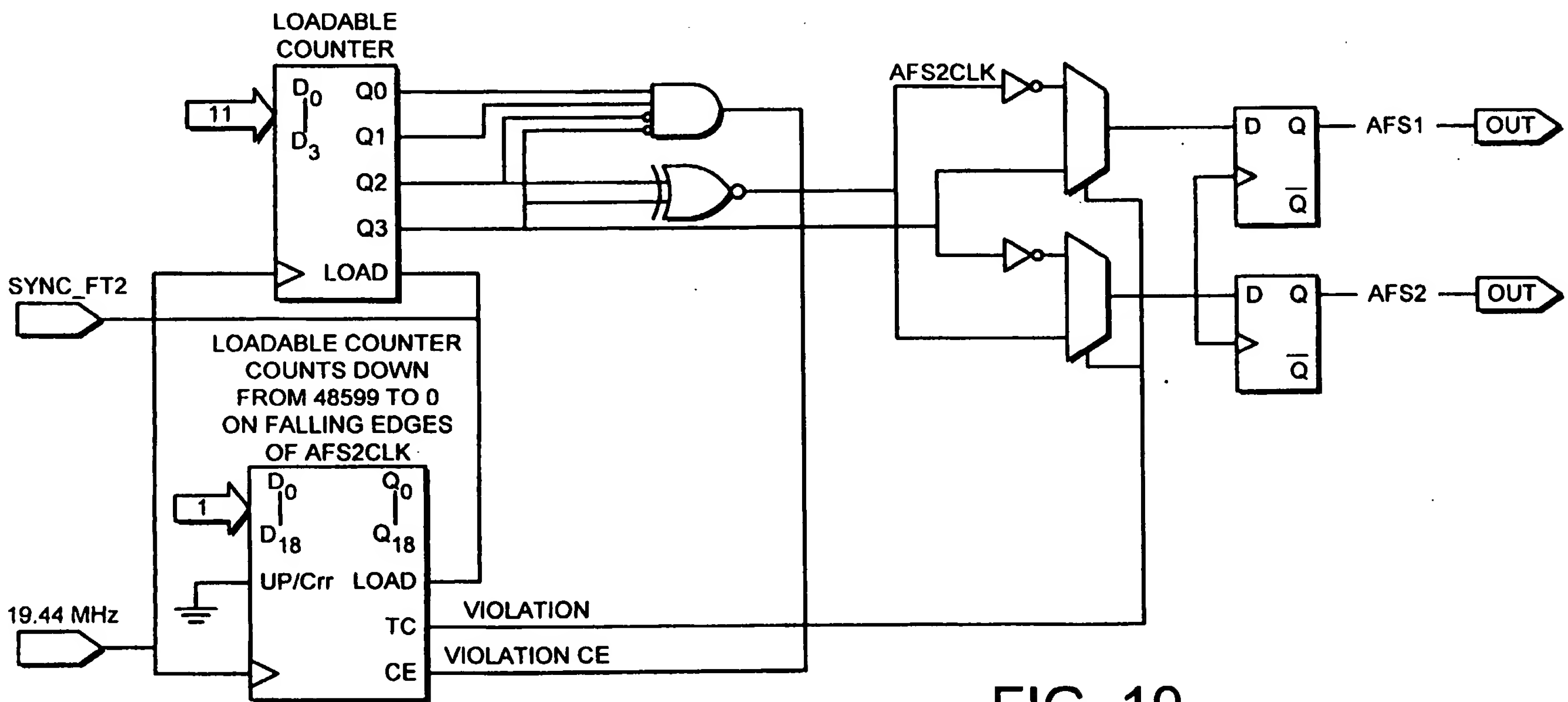

LOADABLE
COUNTER
11
D_0
D_3
Q0
Q1
Q2
Q3
LOAD
SYNC_FT2
LOADABLE COUNTER
COUNTS DOWN
FROM 48599 TO 0
ON FALLING EDGES
OF AFS2CLK
1
D_0
D_{18}
Q_0
Q_{18}
UP/Crr
LOAD
TC
CE
19.44 MHz
VIOLATION
VIOLATION CE
AFS2CLK
D
Q
$\overline{Q}$
AFS1
AFS2
OUT
OUT

FIG. 10